

ADAPT812

Put the power and flexibility of the 68HC812A4 microcontroller to work in your application!



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Adapt812 is based on Motorola's 68HC812A4 16-bit microcontroller. The 68HC12 architecture was carefully designed by Motorola to be highly compatible with the 68HC11, while offering impressive new features and processing power. With many new and powerful instructions and addressing modes, this family offers a very high level of performance for embedded applications, offering expanded memory addressing (to over 5MB), dual SCIs, and key-wakeup capability, making it possible to easily implement complex applications.

In single-chip mode Adapt812 offers 4K EEPROM and 1K RAM. The modular design and dual 50-pin connectors provide dozens of I/O lines, and an on-chip bootloader provides fast, easy downloading via the serial port.

In expanded mode, one of the connectors becomes an expansion bus, designed to mate with a memory card. Available in several configurations, compatible memory cards provide Flash, battery-backed SRAM, a clock/calendar, and a prototyping area for the user's application circuitry.

TECHNICAL SPECIFICATIONS

ADAPT-812

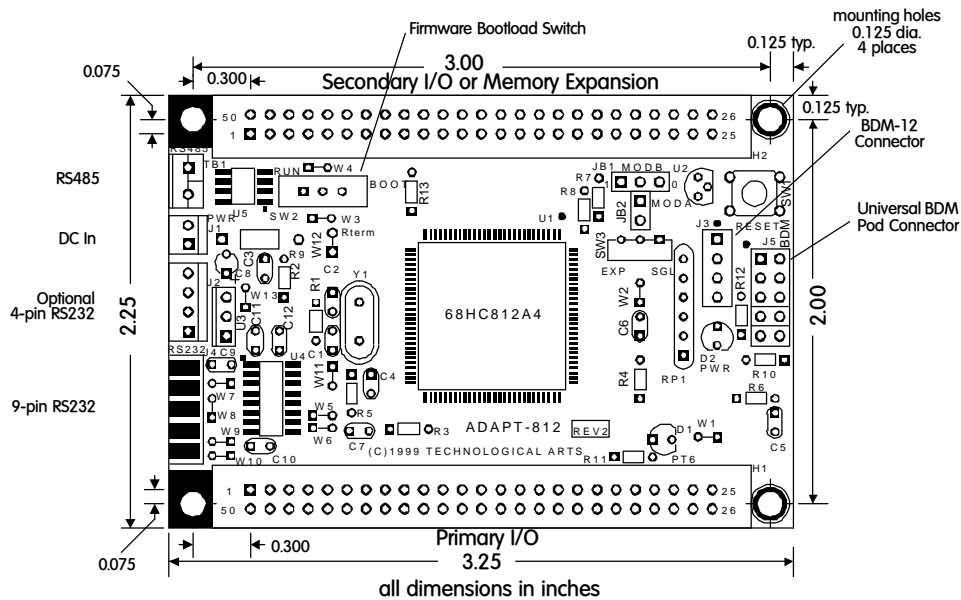
- compact (2.25" x 3.25") modular implementation of the 68HC812A4
- versatile connector configurations support solderless breadboard, prototyping cards, ribbon cable, and vertical or horizontal stacking applications
- primary 50-pin connector for dedicated I/O
- secondary 50-pin connector for additional I/O or memory expansion bus
- memory expandable offboard to 4MB program and 1MB data memory
- 8 MHz bus speed (16 MHz crystal)
- includes both RS232 and RS485 interfaces
- universal 6-pin/10-pin connector for access to Background Debug Mode
- supports BDM pods from multiple vendors
- program in C, BASIC, or assembler
- on-chip bootloader for easy in-circuit programming (BDM pod not required)
- includes full schematic, documentation, and application notes

68HC812A4

- 16-bit microcontroller in 112-pin thin quad flat pack (TQFP) package
- high degree of 68HC11 architecture and instruction set compatibility
- greatly expanded instruction set has DSP & Fuzzy Logic instructions, memory-to-memory transfers, table lookup, min & max value, and more

- all HC11 addressing modes, plus new indexed addressing modes, including accumulator offset indexing, and auto increment/decrement
- high speed operation (8MHz bus speed, using 16 MHz crystal)
- single chip mode operation using internal 4K EEPROM and 1K SRAM
- expanded mode operation supports up to 4MB program memory, 1MB data memory, and 256K extra decodable peripheral/memory space
- non-multiplexed address and data buses
- seven programmable chip selects provided for glueless interface to memories and peripherals
- selectable narrow (8-bit) or wide (16-bit) bus interface
- two enhanced serial communication interface (SCI) ports support any baud rate to 38.4K bps
- multiple I/O port lines, with programmable pullup resistors on most pins
- programmable reduced-drive on all I/O lines
- multiple "key wakeup" port lines for use with keypad (any key pressed wakes up MCU)
- serial peripheral interface (SPI) port
- eight input capture/output compare lines
- versatile 8-channel, 16-bit hardware timer subsystem
- 16-bit pulse accumulator
- high speed 8-channel 8-bit analog-to-digital converters

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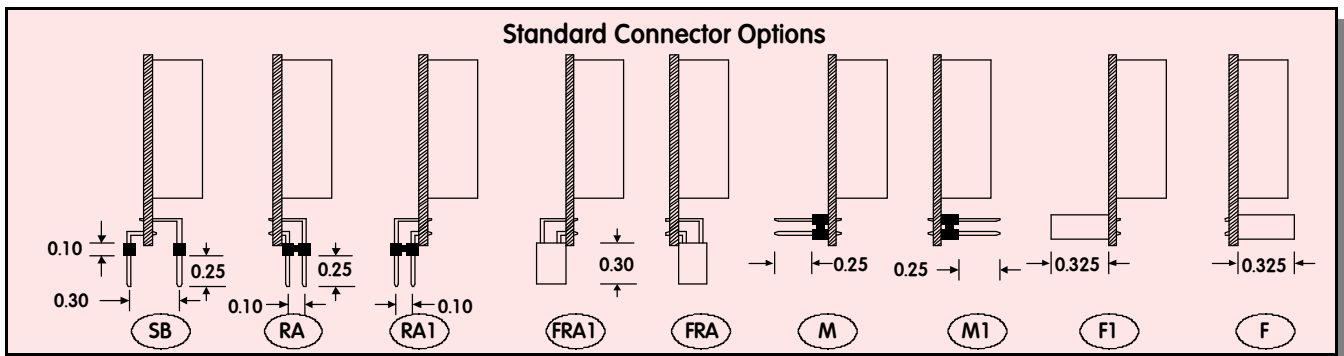


Adapt812 CONNECTOR PINOUTS (REV. 2)

H1				H2			
PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME
① 1	PS4/MISO	50	GROUND	1	DATA15/PC7	50	VCC (+5VDC)
① 2	PS5/MOSI	49	GROUND	2	DATA14/PC6	49	GROUND
① 3	PS6/SCK	48	PS0/RXD0	3	DATA13/PC5	48	CSP1*/PF6
4	PS7/SS*	47	+5VDC	4	DATA12/PC4	47	CSP0*/PF5
5	PS1/TXD0	46	IRQ*	5	DATA11/PC3	46	CSD*/PF4
6	PT7/OC7/PAI	45	XIRQ*	6	DATA10/PC2	45	CS3*/PF3
7	PT6/OC6	44	RESET*	7	DATA9/PC1	44	CS2*/PF2
8	PT5/OC5	43	PE7/ARST	8	DATA8/PC0	43	CS1*/PF1
9	PT4/OC4	42	KWH0	9	DATA7/KWD7	42	CS0*/PF0
10	PT3/OC3	41	KWH1	10	DATA6/KWD6	41	ADDR21/PG5
11	PT2/OC2	40	KWH2	11	DATA5/KWD5	40	ADDR20/PG4
12	PT1/OC1	39	KWH3	12	DATA4/KWD4	39	ADDR19/PG3
13	PT0/OC0	38	KWH4	13	DATA3/KWD3	38	ADDR18/PG2
14	PJ7/KWJ7	37	KWH5	14	DATA2/KWD2	37	ADDR17/PG1
15	PJ6/KWJ6	36	KWH6	15	DATA1/KWD1	36	ADDR16/PG0
16	PJ5/KWJ5	35	KWH7	16	DATA0/KWD0	35	ADDR6/PB6
17	PJ4/KWJ4	34	PS2/RXD1	17	R/W* PE2	34	ADDR7/PB7
18	PJ3/KWJ3	33	PE4/ECLK	18	ECLK/PE4	33	ADDR8/PA0
19	PJ2/KWJ2	32	PS3/TXD1	19	LSTRB*/PE3	32	ADDR9/PA1
20	PJ1/KWJ1	31	VRL	20	ADDR0/PB0	31	ADDR10/PA2
21	PJ0/KWJ0	30	VRH	21	ADDR1/PB1	30	ADDR11/PA3
22	PAD0/AN0	29	PAD4/AN4	22	ADDR2/PB2	29	ADDR12/PA4
23	PAD1/AN1	28	PAD5/AN5	23	ADDR3/PB3	28	ADDR13/PA5
24	PAD2/AN2	27	PAD6/AN6	24	ADDR4/PB4	27	ADDR14/PA6
25	PAD3/AN3	26	PAD7/AN7	25	ADDR5/PB5	26	ADDR15/PA7

NOTES: * indicates active low signal

① pin assignment changed from REV. 1



Module: #AD812M-□-□
 Starter Package: #AD812SP(-□-□)
 (default RA-M connectors unless otherwise specified)