

# ADAPT912

*Put the power of Motorola's  
68HC912B32 microcontroller  
to work in your application!*

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**Adapt912 is a single-chip implementation of the 68HC912B32, providing 32K on-chip Flash, dozens of I/O pins, including SPI, J1850 (BDLC), a 4-channel pulse-width modulator (PWM), and 8-channels 8-bit A-to-D. Now it's possible to easily implement sophisticated and complex applications.**

**As a member of the Adapt12 Modular Prototyping Family, Adapt912 can be combined with prototyping cards in a stacked, end-to-end, or back-plane arrangement. Two standard 50-pin I/O connectors make all the MCU's I/O lines accessible to the user.**

**With on-chip firmware (D-Bug12), downloading and debugging application code can be done via the serial port. By a simple jumper selection, Adapt912 can be used as a BDM pod with any 68HC12 target.**

**The architecture of the 68HC12 is highly compatible with the 68HC11, while offering impressive new features and processing power. With many new and powerful instructions and addressing modes, this chip offers a very high level of performance for embedded applications.**

## TECHNICAL SPECIFICATIONS

### ADAPT-912

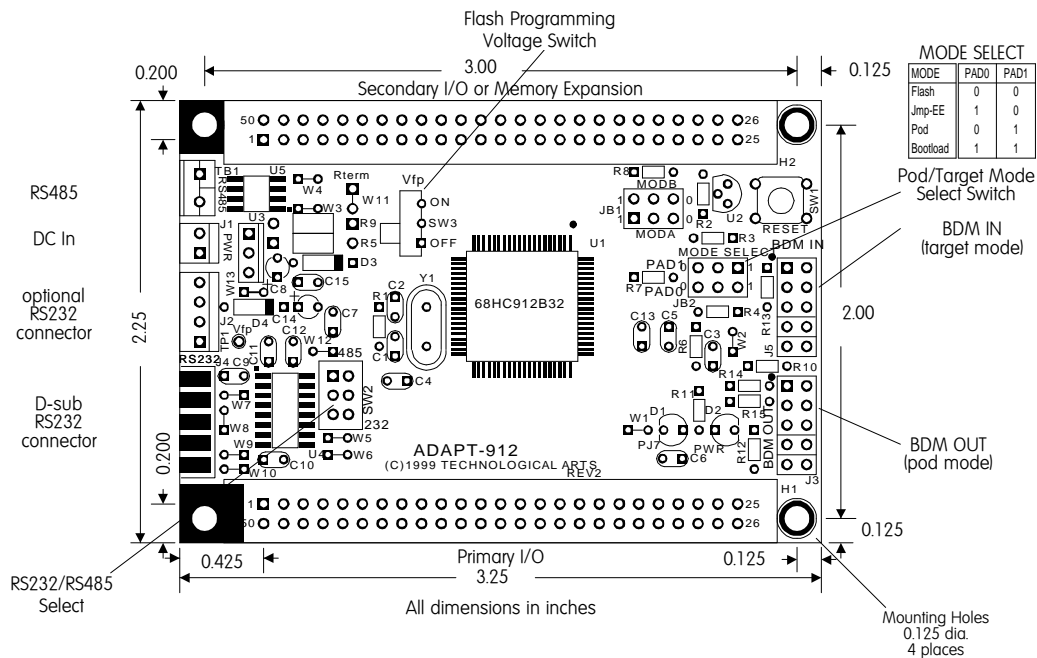
- compact (2.25" x 3.25") modular implementation of the 68HC912B32
- versatile connector options support solderless breadboard, prototyping cards, ribbon cable, or embedded applications
- primary 50-pin connector for dedicated I/O
- secondary 50-pin connector for additional I/O or memory expansion bus
- 8 MHz bus speed (16 MHz crystal)
- includes both RS232 and RS485 interfaces (switch-selectable)
- universal 6-pin/10-pin connector for access to Background Debug Mode
- supports BDM pods from multiple vendors
- also functions as BDM pod for target HC12 board, via BDM Out connector
- program it in C, BASIC, or assembler
- on-chip bootloader for easy in-circuit programming (BDM pod not required)
- includes full schematic, documentation, and application notes

### 68HC912B32

- 16-bit microcontroller in 80-pin quad flat pack (QFP) package
- high degree of 68HC11 architecture and instruction set compatibility
- greatly expanded instruction set has DSP & Fuzzy Logic instructions, memory-to-memory transfers, table lookup, min & max value, and more

- all HC11 addressing modes, plus new indexed addressing modes, including accumulator offset indexing, and auto increment/decrement
- high speed operation (8MHz bus speed, using 16 MHz crystal)
- single chip mode operation using internal 32K Flash, 768 bytes EEPROM, and 1K SRAM
- expanded mode operation supported (64K max.)
- multiplexed address and data buses
- selectable narrow (8-bit) or wide (16-bit) bus interface
- enhanced serial communication interface (SCI) ports support any baud rate to 38.4K bps
- serial peripheral interface (SPI) port
- J1850 Byte Data Link Communications (BDLC) interface
- multiple I/O port lines, with programmable pullup resistors on most pins
- programmable reduced-drive on all I/O lines
- 8-bit, 4-channel PWM, or 16-bit, 2-channel PWM (pulse-width modulator)
- eight input capture/output compare lines
- versatile 8-channel, 16-bit hardware timer subsystem
- 16-bit pulse accumulator
- high speed 8-channel 8-bit analog-to-digital converters
- single-wire background debug mode (BDM) for debugging and code loading
- hardware breakpoints

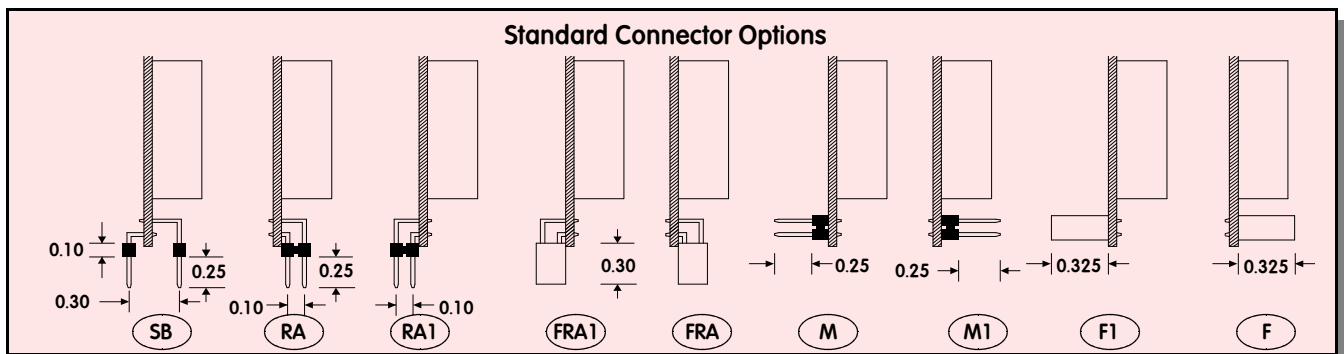
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### ADAPT912 CONNECTOR PINOUTS

H1				H2			
PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	PS4/SDI/MISO	50	GROUND	1	MUX15/PA7	50	VCC (+5VDC)
2	PS5/SDO/MOSI	49	GROUND	2	MUX14/PA6	49	GROUND
3	PS6/SCK	48	PS0/RXD0	3	MUX13/PA5	48	DBE*
4	PS7/SS*	47	+5VDC	4	MUX12/PA4	47	GROUND
5	PS1/TXD0	46	IRQ*	5	MUX11/PA3	46	GROUND
6	PT7/IOC7/PAI	45	XIRQ*	6	MUX10/PA2	45	GROUND
7	PT6/IOC6	44	RESET*	7	MUX9/PA1	44	GROUND
8	PT5/IOC5	43	PE7/DBE*	8	MUX8/PA0	43	VIN
9	PT4/IOC4	42	PDLC0	9	MUX7/PB7	42	VIN
10	PT3/IOC3	41	PDLC1	10	MUX6/PB6	41	VIN
11	PT2/IOC2	40	PDLC2	11	MUX5/PB5	40	VIN
12	PT1/IOC1	39	PDLC3	12	MUX4/PB4	39	RESERVED
13	PT0/IOC0	38	PDLC4	13	MUX3/PB3	38	RESERVED
14	PJ7/PP7	37	PDLC5	14	MUX2/PB2	37	RESERVED
15	PJ6/PP6	36	PDLC6	15	MUX1/PB1	36	RESERVED
16	PJ5/PP5	35	RESERVED	16	MUX0/PB0	35	RESERVED
17	PJ4/PP4	34	PS2	17	R/W* / PE2	34	RESERVED
18	PJ3/PP3/PW3	33	PE4/ECLK	18	ECLK/PE4	33	RESERVED
19	PJ2/PP2/PW2	32	PS3	19	LSTRB*/PE3	32	RESERVED
20	PJ1/PP1/PW1	31	VRL	20	RESERVED	31	RESERVED
21	PJ0/PP0/PW0	30	VRH	21	RESET*	30	RESERVED
22	PAD0/ANO	29	PAD4/AN4	22	MISO	29	RESERVED
23	PAD1/AN1	28	PAD5/AN5	23	MOSI	28	RESERVED
24	PAD2/AN2	27	PAD6/AN6	24	SCK	27	RESERVED
25	PAD3/AN3	26	PAD7/AN7	25	SS*	26	RESERVED

NOTE: \* indicates active low signal



Module: #AD912M-□-□  
 Starter Package: #AD912SP(-□-□)  
 (supplied with RA-M connectors unless otherwise specified)